IN THE CLAIMS:

Claims 1- 10 (canceled).

Claim 11 (previously presented): The device of Claim 21 wherein the gate electrode comprises a metal.

Claim 12 (previously presented): The device of Claim 21 wherein each of the source/drain regions has a depth into the well of about 100 to about 1000 Angstroms.

Claim 13 (previously presented): The device of Claim 21 wherein the source/drain regions comprise amorphous material.

Claims 14-20 (canceled).

Claim 21 (previously presented): A semiconductor device formed on a substrate and comprising:

a well, said well comprising two silicon germanium filled spaces and a remaining portion, said remaining portion of said well not comprising silicon germanium;

a channel region of first conductivity type and being in the well;

a dielectric layer overlying the channel region; and

a gate electrode overlying the dielectric layer;

wherein said two silicon germanium filled spaces comprise respective source/drain regions of second conductivity type, said respective source/drain regions being situated on opposite sides of the channel region.

Claim 22 (previously presented): A semiconductor device formed on a substrate and comprising:

a well;

a channel region of first conductivity type and being in said well;

a dielectric layer overlying said channel region;

a diffusion barrier layer overlying said dielectric layer;

a gate electrode overlying said diffusion barrier layer;

a blocking layer overlying said gate electrode; and

two source/drain regions of second conductivity type formed on opposite sides of said channel region;

wherein each of said dielectric layer, said diffusion barrier layer, and said blocking layer comprise epitaxial layers.

Claim 23 (previously presented): The device of claim 22 wherein said gate electrode comprises silicon germanium.

Claim 24 (previously presented): The device of claim 22 wherein each of said source/drain regions comprises silicon germanium.

Claim 25 (previously presented): The device of claim 22 wherein each of said source/drain regions comprises amorphous silicon germanium.

Claim 26 (previously presented): The device of claim 22 wherein said dielectric layer is selected from the group consisting of oxides of zircon, oxides of titanium, oxides of tantalum, and oxides of hafnium.

Claim 27 (previously presented): The device of claim 22 wherein said blocking layer comprises less than or equal to ten atomic monolayers.

Claim 28 (previously presented): The device of claim 22 wherein said diffusion barrier layer comprises less than or equal to ten atomic monolayers.

Claim 29 (new): A semiconductor device formed on a substrate and comprising:

a well;

a channel region of first conductivity type and being in the well;

a dielectric layer overlying the channel region;

a diffusion barrier layer directly overlying and in contact with the dielectric layer, said diffusion barrier layer being a single layer;

a gate electrode directly overlying and in contact with the diffusion barrier layer, said gate electrode layer comprising a semiconductor material;

a blocking layer overlying the gate electrode;

two source/drain regions of second conductivity type formed on opposite sides of the channel region;

wherein each of the dielectric layer, the diffusion barrier layer, and the blocking layer comprise epitaxial layers.

Claim 30 (new): A semiconductor device formed on a substrate and comprising:

a well;

a channel region of first conductivity type and being in the well;

a dielectric layer overlying the channel region;

a diffusion barrier layer directly overlying and in contact with the dielectric layer, said diffusion barrier layer being a single layer;

a gate electrode directly overlying and in contact with the diffusion barrier layer, said gate electrode layer comprising a semiconductor material;

a blocking layer overlying the gate electrode;

two source/drain regions of second conductivity type formed on opposite sides of the channel region;

wherein the gate electrode comprises silicon germanium.

Claim 31 (new): A semiconductor device formed on a substrate and comprising:

a well;

a channel region of first conductivity type and being in the well;

a dielectric layer overlying the channel region;

a diffusion barrier layer directly overlying and in contact with the dielectric layer, said diffusion barrier layer being a single layer;

a gate electrode directly overlying and in contact with the diffusion barrier layer, said gate electrode layer comprising a semiconductor material;

a blocking layer overlying the gate electrode;

two source/drain regions of second conductivity type formed on opposite sides of the channel region;

wherein each of the source/drain regions comprises silicon germanium.

Claim 32 (new): The device of Claim 31 wherein each of the source/drain regions comprises amorphous silicon germanium.